

REMARKS

Claims 1-32 stand subject to a restriction requirement in the outstanding Official Action. Claim 19 has been amended to depend from claim 1 and therefore claims 1-32 remain in the application.

Attached hereto is a marked-up version of the changes made to the specification and claim(s) by the current amendment. The attached page(s) is captioned "Version With Markings To Show Changes Made."

The Examiner requires restriction between original claims 1-18 directed to a transistor and original claims 19-32 directed to a method of providing a transistor. Applicants elect with traverse the invention of Group I, claims 1-18, drawn to a transistor. However, in the above amendment, applicants have amended claim 19 to be dependent from claim 1, i.e. a method of providing the transistor of claim 1, and therefore believes that claims 19-32 to be properly considered in the present application. Accordingly, claims 1-32 remain in this application.

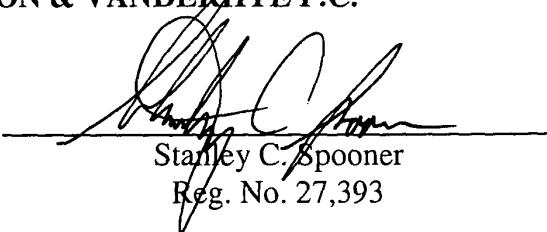
As a result of the above requirement, applicants elect with traverse Group I and believes that claims 19-32, as amended, should now also be considered in Group I.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1-32 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact applicants' undersigned representative.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

19. (Amended) A method of providing [a] the transistor according to claim 1 comprising:

providing a substantially one-dimensional elongate conducting means by providing a first semiconductor substantially surrounded by a second semiconductor material, the elongate conducting means being provided by creating a groove of second semiconductor such that at least one wall of the groove is a substantially planer surface roughly parallel to a crystal plane on which the growth rate of the first semiconductor is substantially zero and subsequently providing the first semiconductor in the groove,

providing a source electrode at a first end region of the conducting means and a drain electrode at a second end region of the conducting means, and

providing at least one further gate electrode in a region of the conducting means.